

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/20/08 has been entered.
2. Claims 1 and 5-8 have been allowed.
3. Claims 2-4, and 9-16 have been cancelled.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with the applicant's representative, Mr. Nock James on 02/29/08.

The abstract has been amended as follows:

Methods and apparatus are ~~disclosed~~ provided that allow an electronic system having a signaling bus with a fault on a signaling conductor to operate at a degraded performance. A block of data is transferred from a first electronic unit to a second

electronic unit over the signaling bus. A transmission sequence sends the block of data using all of the nonfaulty signaling conductors using a minimum number of beats required to complete the transmission.

Reasons for Allowance

5. The following is an examiner's statement of reasons for allowance:

The present invention is directed to:

A method for transmitting a "J" bit block of data from a first electronic unit to a second electronic unit over a signaling bus having "K" signaling conductors, where zero to "K-1" of the signaling conductors is faulty, the method comprising the steps of: identifying faulty and nonfaulty signaling conductors in the signaling bus; setting a fault status of the signaling conductors in the first electronic unit and in the second electronic unit, using information found by the step of identifying faulty and nonfaulty signaling conductors in the signaling bus; determining "F", the number of faulty signaling conductors in the signaling bus; determining "K-F", the number of nonfaulty signaling conductors in the signaling bus; and transmitting the "J" bit block of data over the "K-F" nonfaulty signaling conductors using "J/(K-F)" beats, plus an additional beat if a remainder exists;

the step of transmitting further comprises the steps of:

selecting a "K" bit group of data from the "J" bit block of data; transmitting, on a beat, "K-F" bits of the "K" bit group of data, using the "K-F" nonfaulty conductors;

storing the "F" bits in the "K" bit group that cannot be transmitted, on the beat, due to the "F" faulty conductors in the signaling bus;

repeating the above three steps until all "J" bits of the "J" bit block of data have been selected; and

transmitting the stored "F" bits on one or more additional beats, using one or more of the "K-F" nonfaulty signaling conductors;

the step of storing the "F" bits further comprising the step of shifting at least one bit of the "F" bits into a first end of a shift register; and

transmitting at least one of the bits of the shift register to a nonfaulty signaling conductor.

An apparatus for transmitting a "J" bit block of data from a first electronic unit to a second electronic unit comprising: a first block of data in the first electronic unit holding "J" bits for transmission; storage in the second electronic capable of holding a second block of data having "J" bits; a signaling bus having "K" signaling conductors coupling the first electronic unit to the second electronic unit, "K" greater than one, the signaling bus having one (1) faulty signaling conductors and "K-1" nonfaulty signaling conductors; a diagnostic unit coupled to the first electronic unit and to the second electronic unit capable of identifying the "1" faulty signaling conductors and the "K- 1" nonfaulty signaling conductors on the signaling bus and storing fault identification information in the first electronic unit and in the second electronic unit; [[and]] a driving sequencer in the first electronic unit that, respondent to the fault identification information, transmits

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the "J" bits of data using $J/(K-1)$ beats, plus an additional beat if a remainder exists, using only the "K- 1" nonfaulty conductors; a shift register having "K" bits, configured to receive, during each beat, at a first end of the shift register, a bit directed to the faulty signaling conductor, the shift register, when full, configured to be rotated for a first rotation, during which first rotation, a bit at a second end of the shift register is received at the first end of the shift register; the apparatus configured to, following the first rotation, transmit K-1 bits of the shift register onto the nonfaulty signaling conductors; the shift register further configured to be rotated for a second rotation, during which second rotation, a bit at the second end of the shift register is received at the first end of the shift register; the apparatus configured to, following the second rotation, transmit the remaining untransmitted bit of the "J" bits on a nonfaulty signaling conductor.

The prior arts of record teach a method for transmitting a "J" bit block of data from a first electronic unit to a second electronic unit over a signaling bus having "K" signaling conductors, where zero to "K-1" of the signaling conductors is faulty, the method comprising the steps of: identifying faulty and nonfaulty signaling conductors in the signaling bus; setting a fault status of the signaling conductors in the first electronic unit and in the second electronic unit, using information found by the step of identifying faulty and nonfaulty signaling conductors in the signaling bus; determining "F", the number of faulty signaling conductors in the signaling bus; determining "K-F", the number of nonfaulty signaling conductors in the signaling bus; and transmitting the "J" bit block of data over the "K-F" nonfaulty signaling conductors using $J/(K-F)$ beats,

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plus an additional beat if a remainder exists; the step of transmitting further comprises the steps of: selecting a "K" bit group of data from the "J" bit block of data; transmitting, on a beat, "K-F" bits of the "K" bit group of data, using the "K-F" nonfaulty conductors; storing the "F" bits in the "K" bit group that cannot be transmitted, on the beat, due to the "F" faulty conductors in the signaling bus; repeating the above three steps until all "J" bits of the "J" bit block of data have been selected; and transmitting the stored "F" bits on one or more additional beats, using one or more of the "K-F" nonfaulty signaling conductors. But the prior art of record fail to teach that the step of storing the "F" bits further comprising the step of shifting at least one bit of the "F" bits into a first end of a shift register; and transmitting at least one of the bits of the shift register to a nonfaulty signaling conductor.

Furthermore, the prior arts of record teach an apparatus for transmitting a "J" bit block of data from a first electronic unit to a second electronic unit comprising: a first block of data in the first electronic unit holding "J" bits for transmission; storage in the second electronic capable of holding a second block of data having "J" bits; a signaling bus having "K" signaling conductors coupling the first electronic unit to the second electronic unit, "K" greater than one, the signaling bus having one (1) faulty signaling conductors and "K-1" nonfaulty signaling conductors; a diagnostic unit coupled to the first electronic unit and to the second electronic unit capable of identifying the "1" faulty signaling conductors and the "K- 1" nonfaulty signaling conductors on the signaling bus and storing fault identification information in the first electronic unit and in the second

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electronic unit; [[and]] a driving sequencer in the first electronic unit that, respondent to the fault identification information, transmits the "J" bits of data using " $J/(K-1)$ " beats, plus an additional beat if a remainder exists, using only the "K- 1" nonfaulty conductors. But the prior arts of record fail to teach a shift register having "K" bits, configured to receive, during each beat, at a first end of the shift register, a bit directed to the faulty signaling conductor, the shift register, when full, configured to be rotated for a first rotation, during which first rotation, a bit at a second end of the shift register is received at the first end of the shift register; the apparatus configured to, following the first rotation, transmit K-1 bits of the shift register onto the nonfaulty signaling conductors; the shift register further configured to be rotated for a second rotation, during which second rotation, a bit at the second end of the shift register is received at the first end of the shift register; the apparatus configured to, following the second rotation, transmit the remaining untransmitted bit of the "J" bits on a nonfaulty signaling conductor.

Hence, the prior arts of record fail to anticipate or render obvious the claimed inventions. Thus claims 1, 5-7 and 8 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10:30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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02/27/08

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